NCP1840

High Current, 8-Output LED Driver

The NCP1840 is a general purpose LED driver with the ability to drive up to eight LEDs. Each of the eight driver currents is fully programmable, each utilizing a 5−bit current DAC. The current can be turned on or off using a programmable 6−bit counter. The full−scale current of all eight current DACs is set by an external resistor on the R_IDAC pin. The quad mode charge pump allows the use of higher forward voltage LEDs while maintaining a low ⌣3.4 V operating battery voltage.

Features

- Programmable, Individual Output PWM Control with 6−Bit Counter
- (8) 30 mA Universal Current Sources with 5−Bit Programmable Logarithmic Brightness Control
- Serial Interface for Convenient Programming
- Small 20−Lead, 4 mm x 4 mm QFN Package
- Single External Resistor Used to Set Full−Scale Range on All 8 Outputs
- Quad Mode (1X, 1.33X, 1.5X and 2X) Charge Pump for Higher Forward−Voltage LEDs (e.g. 4.1 V)
- Power−On−Reset (POR)
- These are Pb−Free Devices

Typical Applications

- Notebook Battery LED Indicator
- “True Green” LED Applications

QFN20
CASE 485E

MARKING DIAGRAM

xxxxxx	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

NCP1840 Device	Package	Shipping†
NCP1840Q8A6MNG	QFN20 (Pb−Free)	TBD Units / Rail
NCP1840Q8A6MNTWG	QFN20 (Pb−Free)	TBD / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

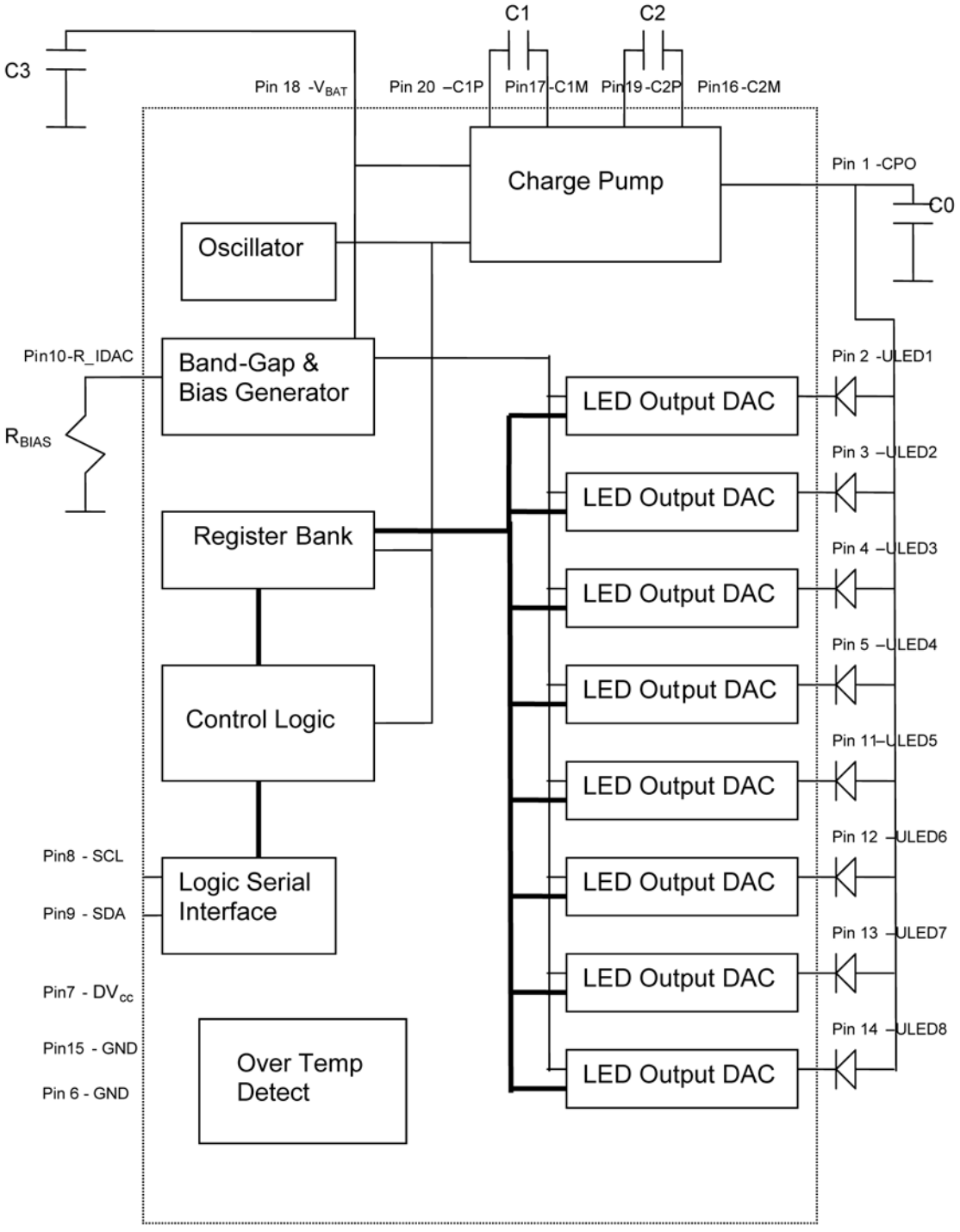


Figure 1. Block Diagram and Typical Application

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	CP0	Charge pump output used as power supply to the LEDs. Should have a 2.2 μF ceramic capacitor (X5R or X7R) connected to ground.
2 to 5; 11 to 14	ULED1 to ULED8	Sink current output. Current value, PWM, blinking and gradation programmable through the serial interface
6	GND	Ground connection. Should be connected along with the “ground pad” to the board ground plane.
7	DV_{CC}	Supply input for the digital circuitry. Should have a 1 μF ceramic capacitor (X5R or X7R) connected to ground.
8	SCL	Serial interface clock input. Logic levels referenced to DV_{CC}
9	SDA	Serial interface data input/output. Logic levels referenced to DV_{CC}
10	R_IDAC	An external 10.25 kΩ resistor connected to ground defines the reference current used to set the current DACs connected to the ULED outputs.
15, (21)	GND	Ground connection. Should be connected along with the “ground pad” to the board ground plane.
16, 17, 19, 20	C2M, C1M, C2P, and C1P	Charge pump flying capacitor connections. A 1 μF ceramic capacitor (X5R or X7R) should be connected from C1P to C1M. A 1 μF ceramic capacitor (X5R or X7R) should be connected from C2P to C2M.
18	V_{BAT}	Supply for the charge pump and analog circuitry. Should have a 2.2 μF low ESR ceramic capacitor connected to ground.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 3)	V_{in}	−0.3 to DV_{CC} + 0.3	V
Output Voltage Range (Note 3)	V_{out}	−0.3 to DV_{CC} + 0.3	V
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−40 to 150	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 1)	ESD_{MM}	175	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 2)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
3. These levels apply to pins SCL and SDA.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, 20L NQFP, 4 x 4 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	66.7	°C/W

OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_f	LED forward voltage			4.1	V	
V_{BAT}	Battery operating voltage	3.3	3.42	5.5	V	
DV_{CC}	Digital Supply Voltage	3.3	3.42	3.6	V	
I_{DVCC}	Digital Supply Current	2.0	2.35	3.10	mA	(Note 4)
$I_{DVCC-LOQ}$	Digital Supply Current – Low Power Mode	0.5	< 1	2	μA	(Note 6)
I_{VBATT}	Battery Supply Current	450	520	750	μA	(Note 4)
$I_{VBATT-LOQ}$	Battery Supply Current – Low Power Mode	0.4	< 1	3.5	μA	(Note 6)
$I_{LED}(31)$	Full−Scale LED Current	28	30	34.5	mA	(Note 5)
$I_{LED}(0)$	Minimum LED Current	0.81	0.85	0.95	mA	(Note 5)
	LED−to−LED Matching		4	6.9	%	(Note 7)
T_A	Ambient Temperature	−40	27	85	°C	

4. All LED outputs off, Charge Pump in 1X Mode, no I^2C Communication.
5. With external R_IDAC = 10.25 kΩ.
6. Part enters Low Power Mode around 5 ms after all LED outputs are “off” and there is no I^2C communication. Communication to the part resumes normal operation in less than 1 ms.
7. For T = −40°C max LED−to−LED matching limit is 7.5%.

I^2C INTERFACE

The NCP1840 is programmed through an I^2C interface. The communication takes place with serial bytes sharing the same I^2C frame. The NCP1840 is a slave only part, data can be written to or read from the part. The max speed clock for the serial interface is 400 kHz. I^2C pins SCL and SDA require external pull-up resistors around 1.3 kΩ.

WRITE PROTOCOL USED BY NCP1840:

1	7	1	1	3	5	1	8	1	1
S	Part Address	W	A	Control Bits	Register Address	A	Register Data	A	P

S = Start Condition, W = Write, A = Acknowledge, P = Stop Condition

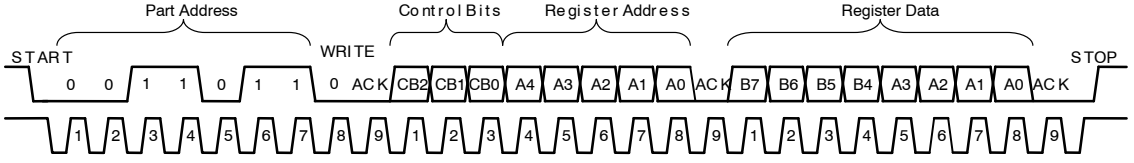


Figure 2.

READ PROTOCOL USED BY NCP1840:

1	7	1	1	3	5	1	8	7	1	1	8	1	1
S	Part Address	W	A	Control Bits	Register Address	A	S	Part Address	R	A	Register Data Out	$\overline{A}$	P

S = Start Condition, W = Write, R = Read, A = Acknowledge, $\overline{A}$ =No Acknowledge, P = Stop Condition

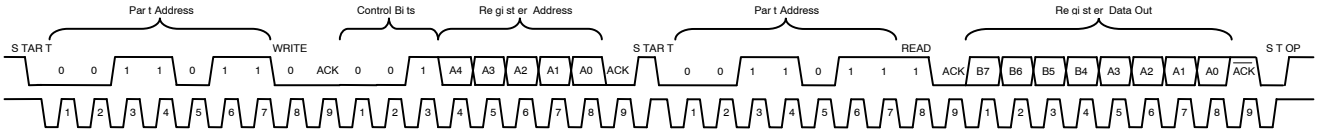


Figure 3.

CONTROL BITS: A

CB2	CB1	CB0	Function
0	0	0	Turn ULEDx ON/OFF according to data programmed to ULED1-8 OUTPUT CONTROL REG
0	0	1	Programming registers. There will be a third byte with data for the address defined by A[4:0]
0	1	0	Programming registers. Turn the outputs active at the end of the third byte.
0	1	1	Program ALL Current Level Registers with third byte data value
1	0	0	Program ALL PWM Registers with third byte data value
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

REGISTER ADDRESS:

A4	A3	A2	A1	A0	ADD-Dec	ADD-Hex	Function
0	0	0	0	0	0	0	ULED1 – current level register address
0	0	0	0	1	1	1	ULED2 – current level register address
0	0	0	1	0	2	2	ULED3 – current level register address
0	0	0	1	1	3	3	ULED4 – current level register address
0	0	1	0	0	4	4	ULED5 – current level register address
0	0	1	0	1	5	5	ULED6 – current level register address
0	0	1	1	0	6	6	ULED7 – current level register address
0	0	1	1	1	7	7	ULED8 – current level register address
0	1	0	0	0	8	8	ULED1 – PWM register address
0	1	0	0	1	9	9	ULED2 – PWM register address
0	1	0	1	0	10	A	ULED3 – PWM register address
0	1	0	1	1	11	B	ULED4 – PWM register address
0	1	1	0	0	12	C	ULED5 – PWM register address
0	1	1	0	1	13	D	ULED6 – PWM register address
0	1	1	1	0	14	E	ULED7 – PWM register address
0	1	1	1	1	15	F	ULED8 – PWM register address
1	0	0	0	0	16	10	ULED 1-8 output control register address
1	0	0	0	1	17	11	Main Status register

REGISTER DESCRIPTION

1. ULEDx – CURRENT LEVEL REGISTER

DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	CODE(DEC)	CURRENT LEVEL
X	X	X	0	0	0	0	0	0	0.85 mA
X	X	X	0	0	0	0	1	1	0.95 mA
X	X	X	0	0	0	1	0	2	1.06 mA
X	X	X	0	0	0	1	1	3	1.19 mA
X	X	X	0	0	1	0	0	4	1.34 mA
X	X	X	0	0	1	0	1	5	1.50 mA
X	X	X	0	0	1	1	0	6	1.69 mA
X	X	X	0	0	1	1	1	7	1.89 mA
X	X	X	0	1	0	0	0	8	2.12 mA
X	X	X	0	1	0	0	1	9	2.38 mA
X	X	X	0	1	0	1	0	10	2.67 mA
X	X	X	0	1	0	1	1	11	3.00 mA
X	X	X	0	1	1	0	0	12	3.37 mA
X	X	X	0	1	1	0	1	13	3.78 mA
X	X	X	0	1	1	1	0	14	4.24 mA
X	X	X	0	1	1	1	1	15	4.76 mA
X	X	X	1	0	0	0	0	16	5.34 mA
X	X	X	1	0	0	0	1	17	5.99 mA
X	X	X	1	0	0	1	0	18	6.72 mA
X	X	X	1	0	0	1	1	19	7.54 mA
X	X	X	1	0	1	0	0	20	8.46 mA
X	X	X	1	0	1	0	1	21	9.49 mA
X	X	X	1	0	1	1	0	22	10.64 mA
X	X	X	1	0	1	1	1	23	11.94 mA
X	X	X	1	1	0	0	0	24	13.40 mA
X	X	X	1	1	0	0	1	25	15.07 mA
X	X	X	1	1	0	1	0	26	16.87 mA
X	X	X	1	1	0	1	1	27	18.93 mA
X	X	X	1	1	1	0	0	28	21.24 mA
X	X	X	1	1	1	0	1	29	23.83 mA
X	X	X	1	1	1	1	0	30	26.74 mA
X	X	X	1	1	1	1	1	31	30.00 mA

NOTE: The max 30 mA is for an external R_IDAC = 10.25 kΩ. The range of R_IDAC is from 10.25 KΩ to 20.5 kΩ. If the external R_IDAC = 20.5 kΩ, the max current would be 15 mA.

X = Don't Care.

2. ULEDx – PWM REGISTER

DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	PWM
X	X	T5	T4	T3	T2	T1	T0	6 bit programmable duty cycle

The initial target for LED period is ~2 kHz – If this period is used, a PWM code 1_{dec} would give an "ON" duty cycle of ~7.937 μs in a period of 500 μs. Code 62_{dec} would have an "ON" duty cycle equal to 492.0635 μs for a period of 500 μs. Finally a code 63_{dec} would have an "ON" duty cycle equal to 500 μs in a period of 500 μs or continuously "ON".

3. ULED1−8 OUTPUT CONTROL REGISTER

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
0	ULED8 off	ULED7 off	ULED6 off	ULED5 off	ULED4 off	ULED3 off	ULED2 off	ULED1 off
1	ULED8 on	ULED7 on	ULED6 on	ULED5 on	ULED4 on	ULED3 on	ULED2 on	ULED1 on

NOTE: Any unused ULED output should not be turned "ON".

4. MAIN STATUS REGISTER

DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
0	0	0	0	0	0 = Normal Operation	0	0 = Normal Operation
0	0	0	0	0	1 = Low Power Mode	0	1 = Over Temperature

SERIAL INTERFACE TIMING INFORMATION

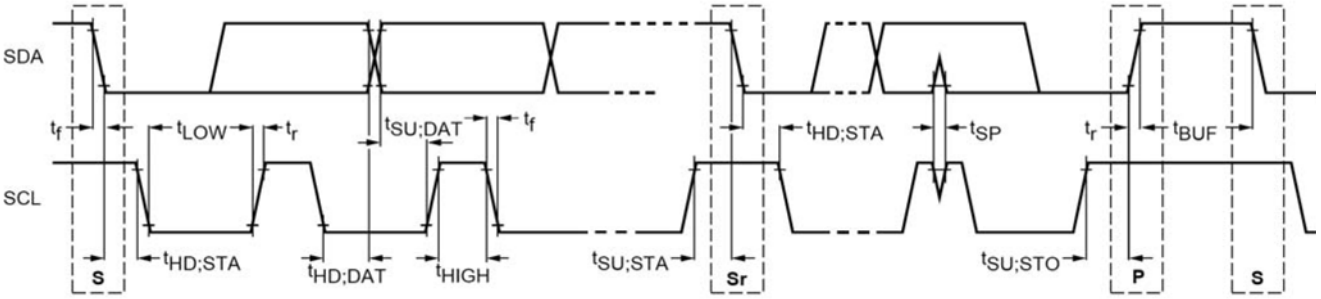


Figure 4.

Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	–	400	kHz
Hold time for Start condition	$t_{HD;STA}$	0.6		μS
LOW Period of SCL Clock	t_{LOW}	1.3		μS
High Period of SCL Clock	t_{HIGH}	0.6		μS
Setup time for Start condition	$t_{SU;STA}$	0.6		μS
Data hold time	$t_{HD:DAT}$		0.9	μS
Data setup time	$t_{SU;DAT}$	100		μS
Rise time	t_r	10	300	nS
Fall time	t_f	10	300	nS
Setup time for Stop condition	$t_{SU;STO}$	0.6		μS
Time between Stop and Start	t_{BUF}	1.3		μS
Capacitive load for each bus line	C_L		200	pF

OVER TEMPERATURE SHUTDOWN

The Over Temperature Shutdown circuit will detect an over temperature condition in the chip. Once the over temperature is detected, all LED outputs and the Charge Pump will be turned off and bit DATA0 on register 17_{dec} will be set to logic one. This register can be read through the serial interface. If the over temperature condition goes away, the bit DATA0 on register 17_{dec} will be automatically reset to a logic zero and the part will resume normal operation. The target trip point for the over temperature shutdown is 130°C to 163°C.

MAXIMUM PACKAGE POWER DISSIPATION

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

NCP1840 LAYOUT GUIDELINES

The NCP1840 requires a low-inductance ground.
Charge pump capacitors C0, C1 and C2 and decoupling capacitor CBAT should be as close to the part as possible.

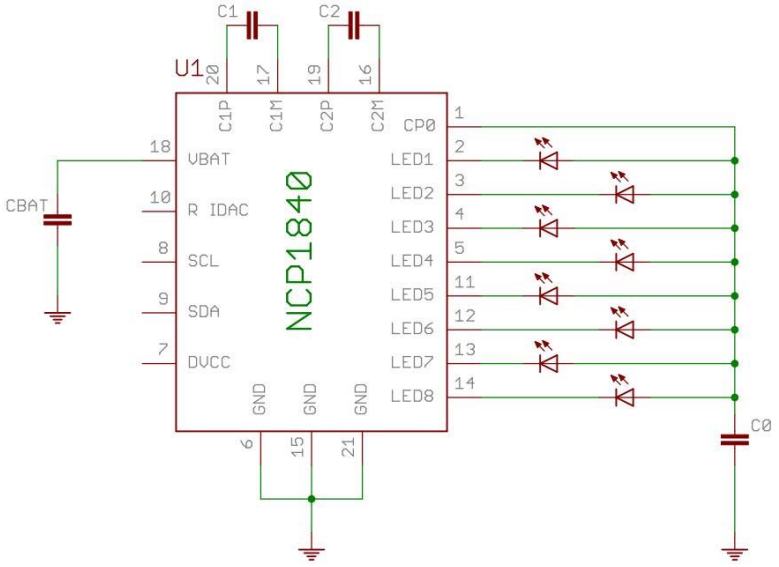


Figure 5. NCP1840 Schematic

GROUND CONNECTION:

Connect pin 6 and pin 15 to the “ground pad” of the IC. (See Figure 6)
Place vias, on the “ground pad”, connecting the GND of the IC directly to the ground plane. (See Figure 6)

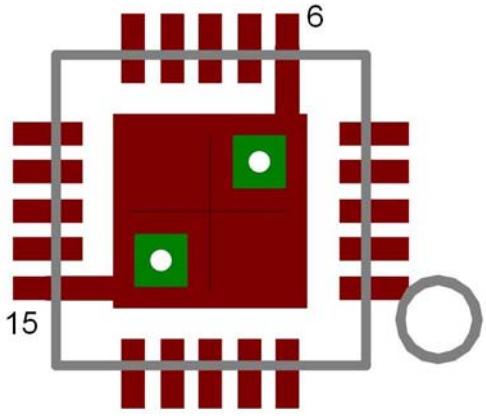


Figure 6. Ground Connection

CHARGE PUMP CAPACITORS: C_0, C_1, C_2, AND C_{BAT}

1. Use good-quality X5R or X7R ceramic capacitors for C_0, C_1, C_2, and C_{BAT}.
2. Connect the positive end of C_0, the output of the charge pump, as close to the IC as possible to ensure charge pump regulation stability. Connect the negative end of the capacitor to GND pin 6, pin 15, or the GND pad. (See Figure 7)
3. Place capacitors C_1 and C_2, the charge pump flying capacitors, and C_{BAT}, the supply voltage for the charge, as close to the IC as possible, minimizing the trace length. (See Figure 7)

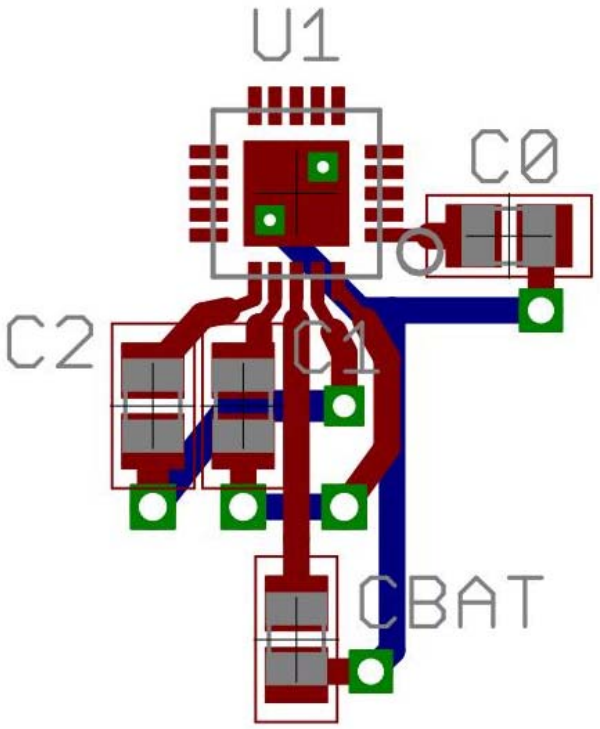
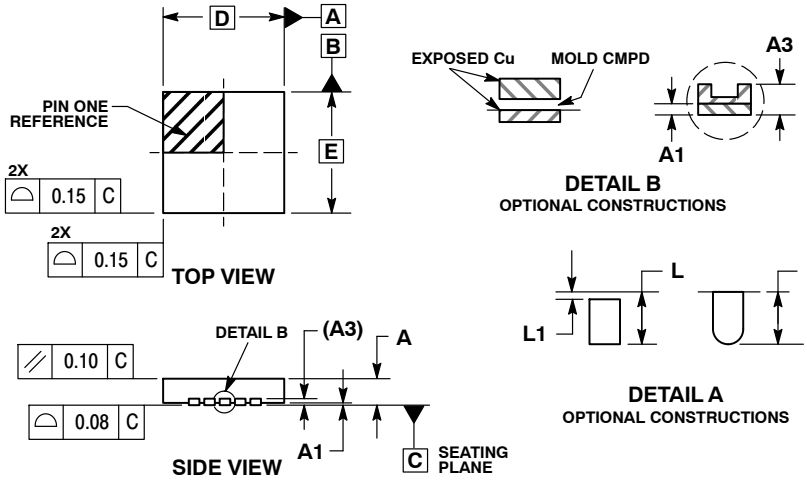


Figure 7. C_0, C_1, C_2, and C_{BAT} layout

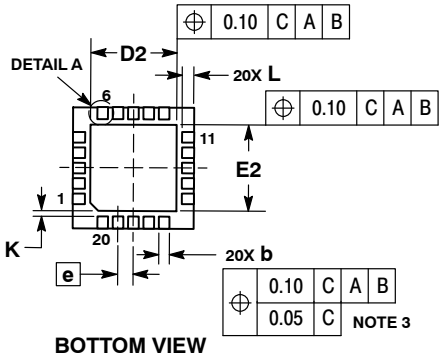
PACKAGE DIMENSIONS

QFN20, 4x4, 0.5P
CASE 485E−01
ISSUE B

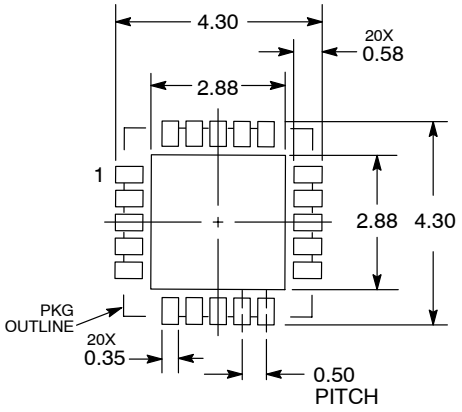


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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